SiGe based low temperature electronics for lunar applications

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Key Challenges

- **Present paradigm**
  - **Use “Warm Electronic Box”**
  - **Use traditional electronics**
  - **Use traditional RTG**
- **New paradigm**
  - **“No Warm Electronics Box”**
  - **Ultra low power and low noise, low temperature instrument quality electronics**
  - **Mini RTG + low temperature rechargeable batteries for burst power**

Key Challenges

- −180°C temperature
  - Can electronics operate at −180°C *Yes*
  - Can we make ultra low power instrumentation quality electronics *TBD*
- Power sources and energy storage technology
  - What are the technology options for powering a science craft
  - What are the alternative technologies for low temperature energy storage

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Silicon-Germanium as an Enabling Technology for Extreme Environment Electronics

John D. Cressler

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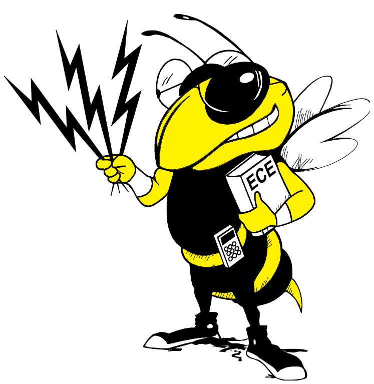

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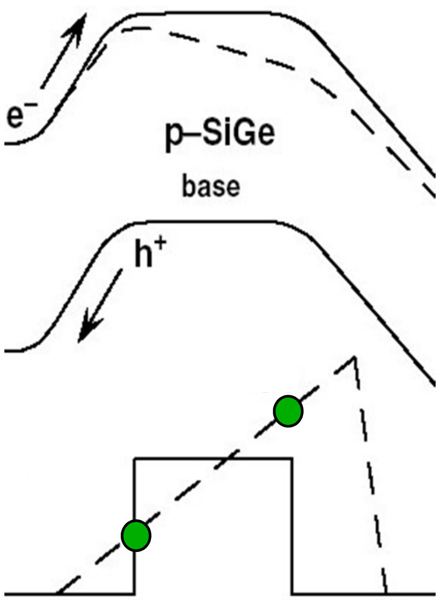
Cryogenic Operation of SiGe HBTs

SiGe HBTs for Cryo-T

The Idea: **Put Graded Ge Layer into the Base of a Si BJT**

Primary Consequences:

- **smaller base bandgap increases electron injection** **(β⬆)**
- **field from graded base bandgap decreases base transit time** **(f_T⬆)**
- **base bandgap grading produces higher Early voltage** **(V_A⬆)**



$$\left.\frac{\beta_{SiGe}}{\beta_{Si}}\right|_{V_{BE}} \equiv \Xi = \left\{ \frac{\tilde{\gamma}\,\tilde{\eta}\,\Delta E_{g,Ge}(grade)/kT\; e^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}} \right\}$$

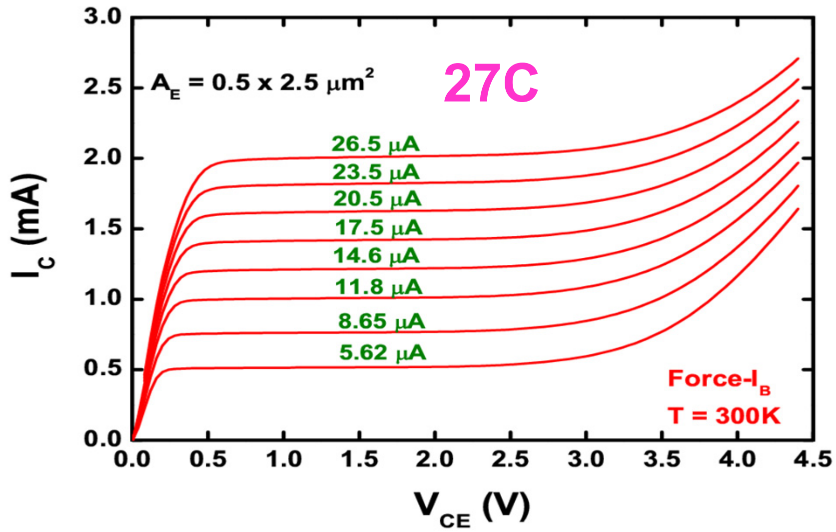
$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\tilde{\eta}}\,\frac{kT}{\Delta E_{g,Ge}(grade)}\left\{1 - \frac{kT}{\Delta E_{g,Ge}(grade)}\left[1 - e^{-\Delta E_{g,Ge}(grade)/kT}\right]\right\}$$

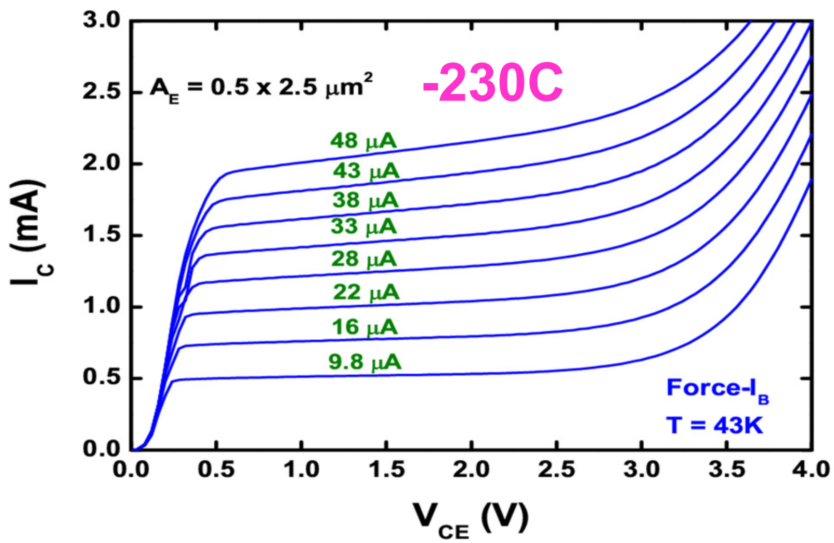
$$\left.\frac{V_{A,SiGe}}{V_{A,Si}}\right|_{V_{BE}} \equiv \Theta \simeq e^{\Delta E_{g,Ge}(grade)/kT}\left[\frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT}\right]$$

All kT Factors Are Arranged to Help at Cryo-T!

SiGe HBTs at Cryo-T

dc





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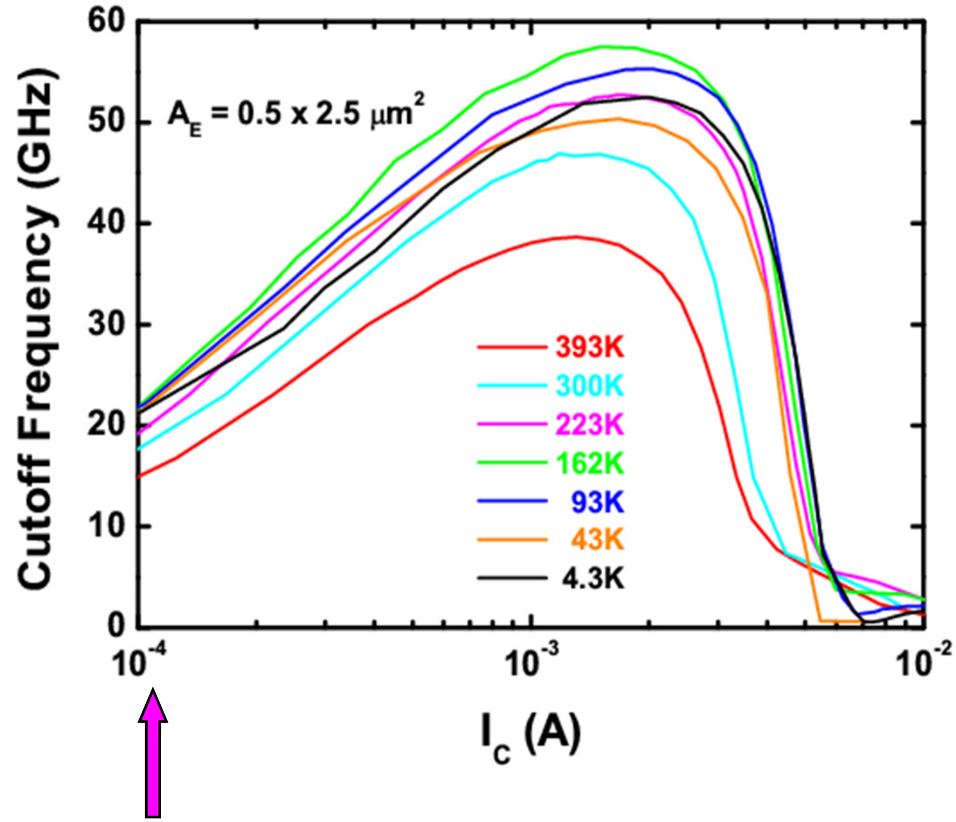


SiGe Exhibits Very High Speed at Very Low Power!

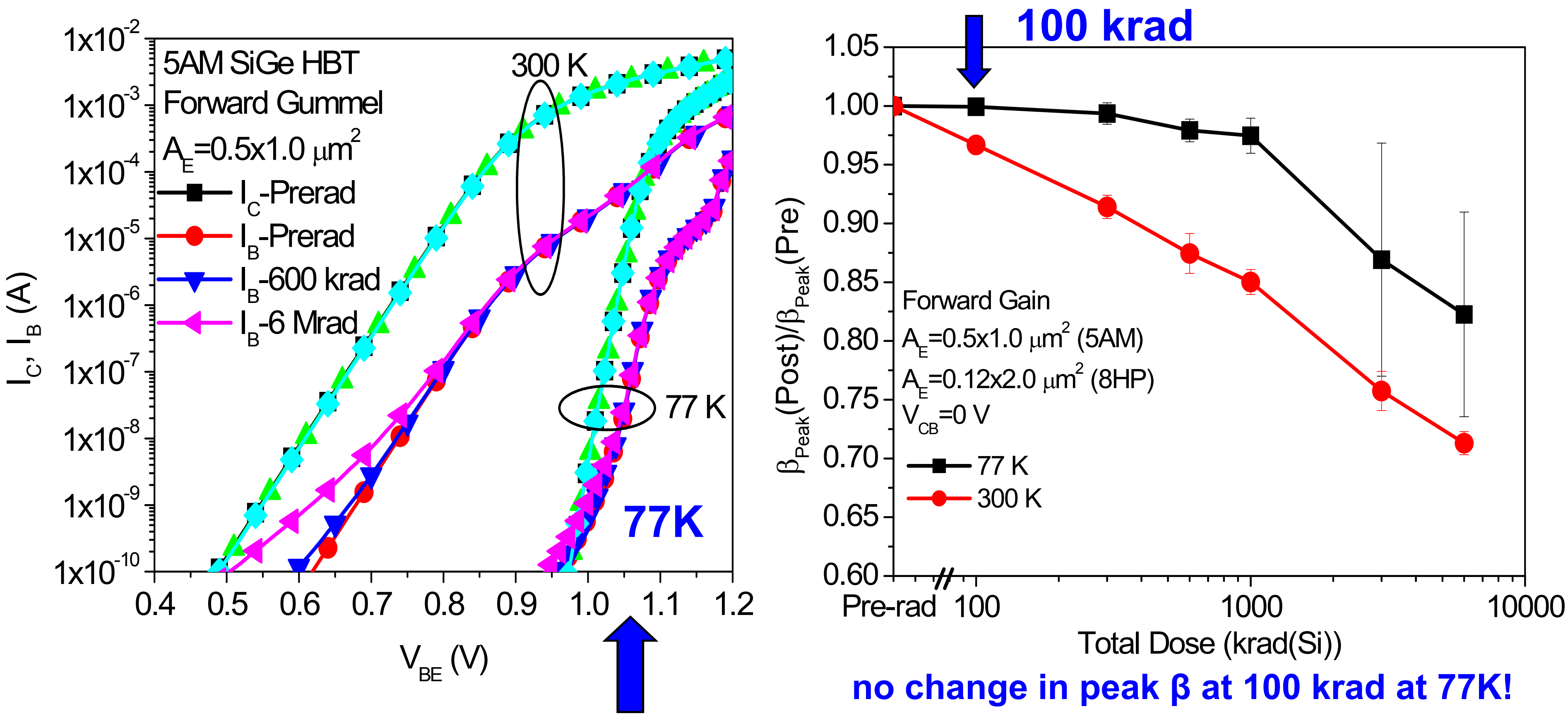
First Generation SiGe HBT

Cryo-T Radiation

First 77K Proton Irradiation Experiment in SiGe Technology

- 63 MeV protons at UC Davis

- **Radiation Damage Smaller at 77K Than at 300K (great news!)**

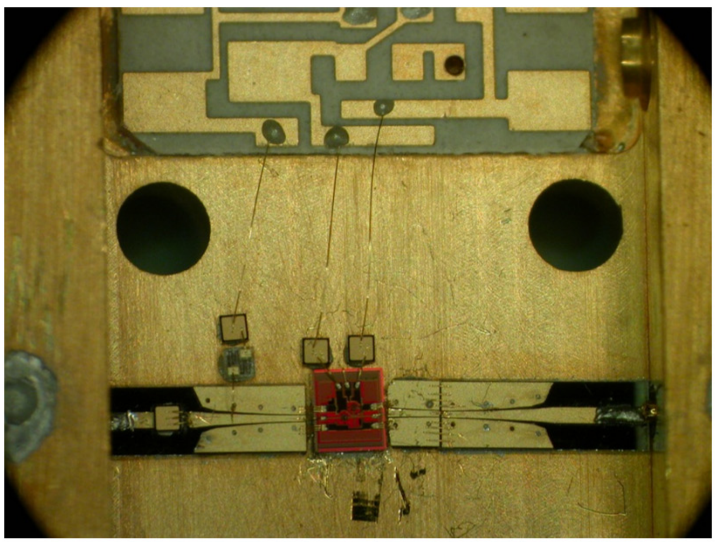


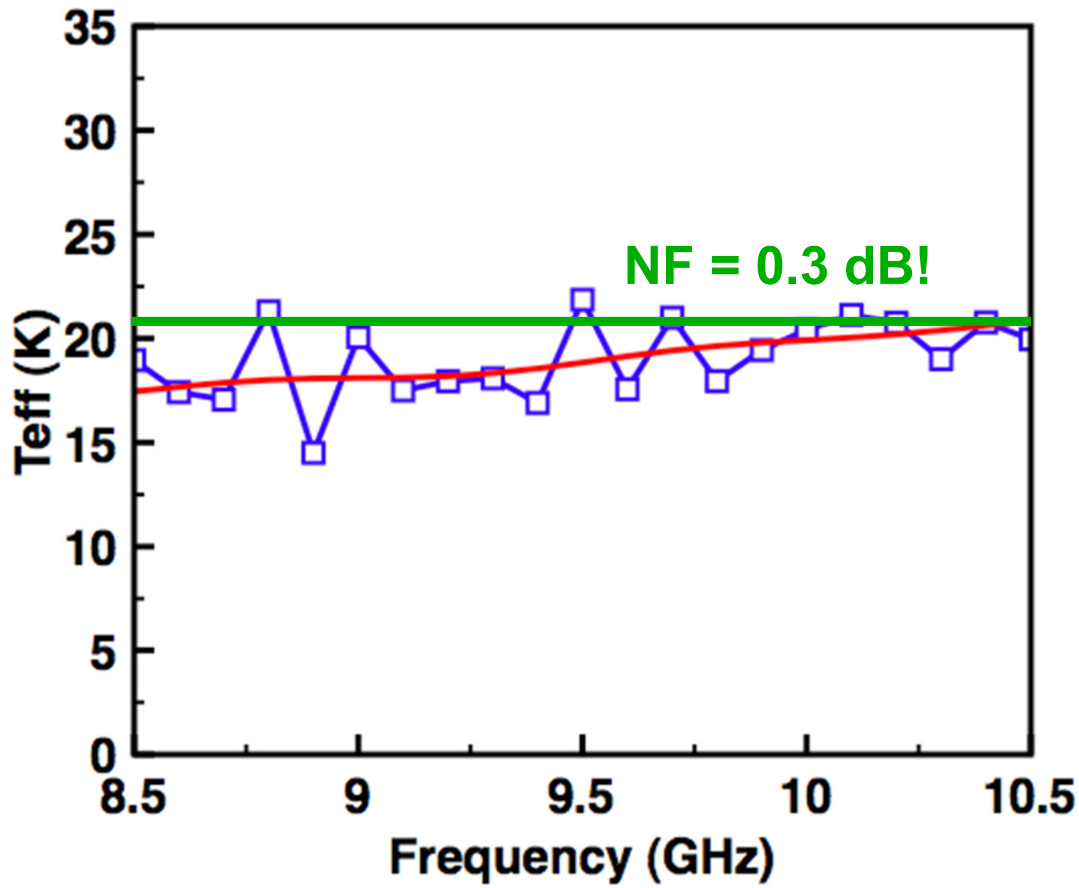
no change in peak β at 100 krad at 77K!

Cryogenic SiGe LNAs

X-band LNA Operation at 15 K (Not Yet Optimized!)

- T_{eff} < 20 K (noise T)
- NF < 0.3 dB
- Gain > 20 dB
- *dc* power < 2 mW





Collaboration with S. Weinreb, Cal Tech

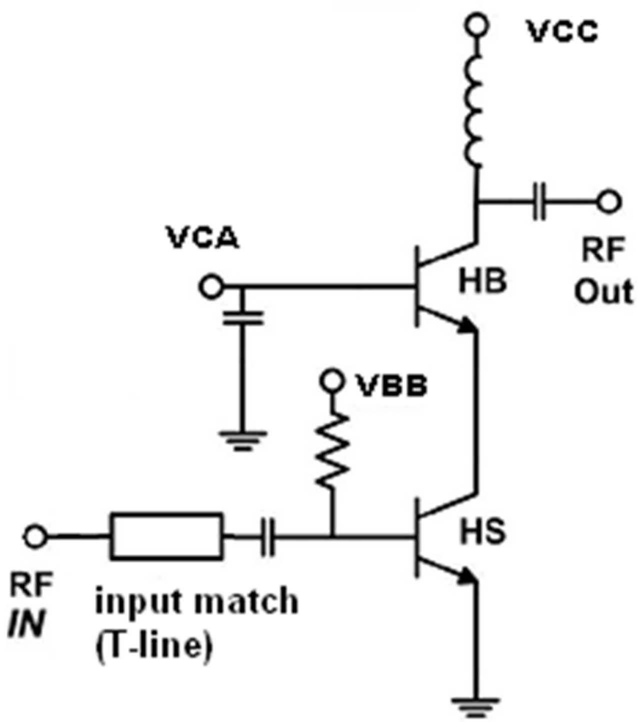
This SiGe LNA is also Rad-Hard!

Aggressive Cascode X-band SiGe PA

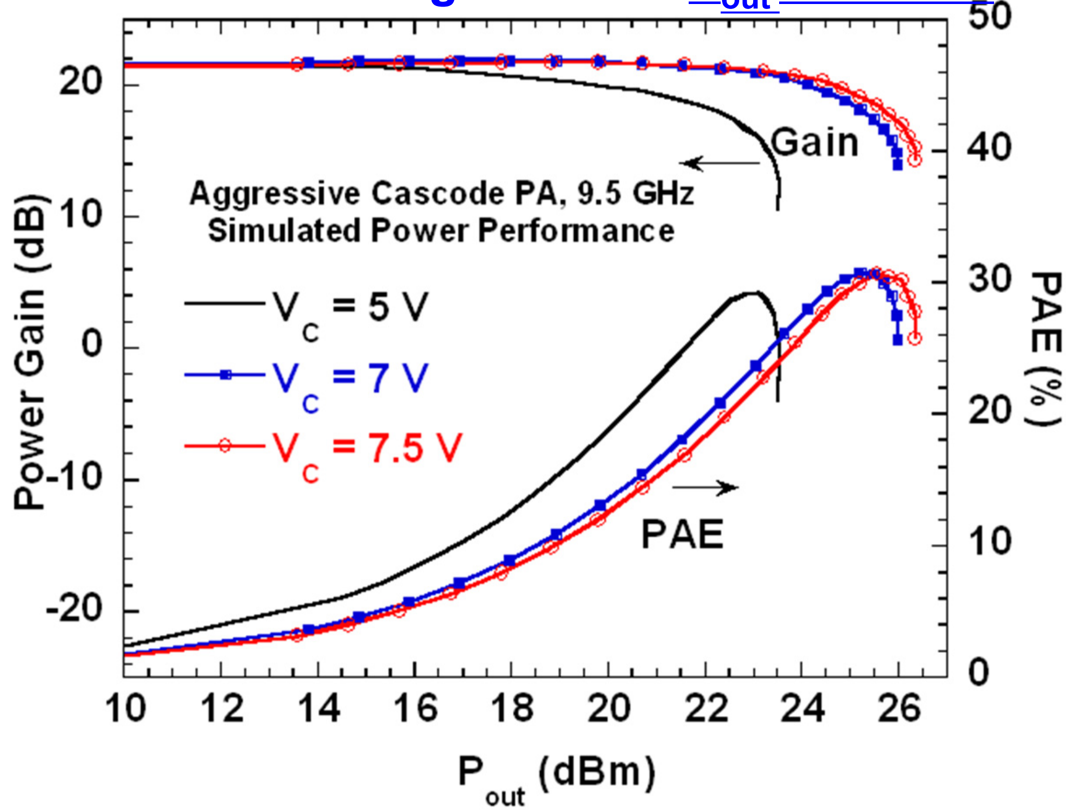
- Current ¼-W SiGe X-band solution (5V): 32 parallel devices
- Can this P_{out} be achieved with a smaller (20 dBm) PA core?

→ Design Cascode PA Using Aggressive V_C Bias

Single-stage Cascode PA Schematic: ($0.12 \times 18 um^2$ HS → $0.6 \times 18 um^2$ HB) x8



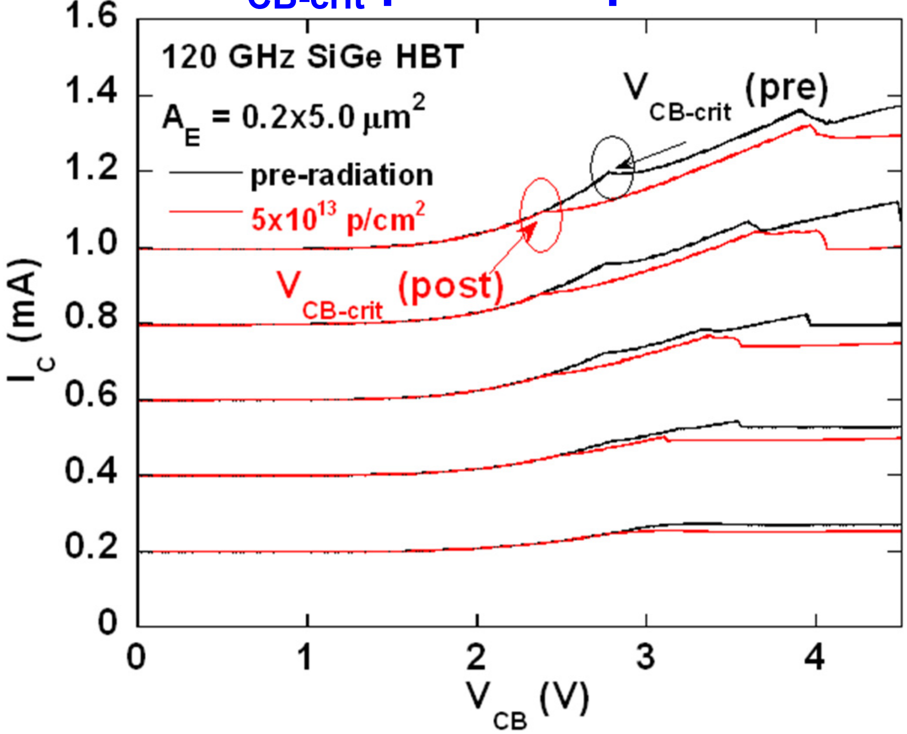
Power Simulations With Aggressive Collector Voltage Bias: → P_{out} > 24 dBm



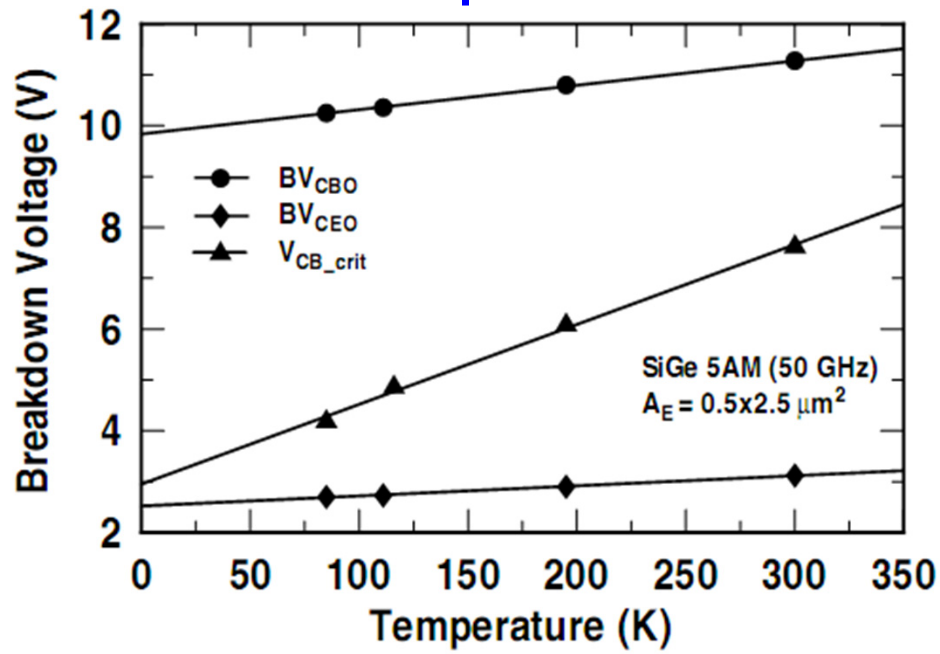
SiGe BV - Extreme Environments

- Both radiation and low T degrade the CB SOA

CB – forced I_E measurement $V_{CB\text{-}crit}$ pre- and post-rad:



Breakdown voltage across temperature:



[21] C. Zhu et al. "Assessing reliability issues in cryogenically-operated SiGe HBT's," IEEE BCTM, pp. 41–44, 2005.

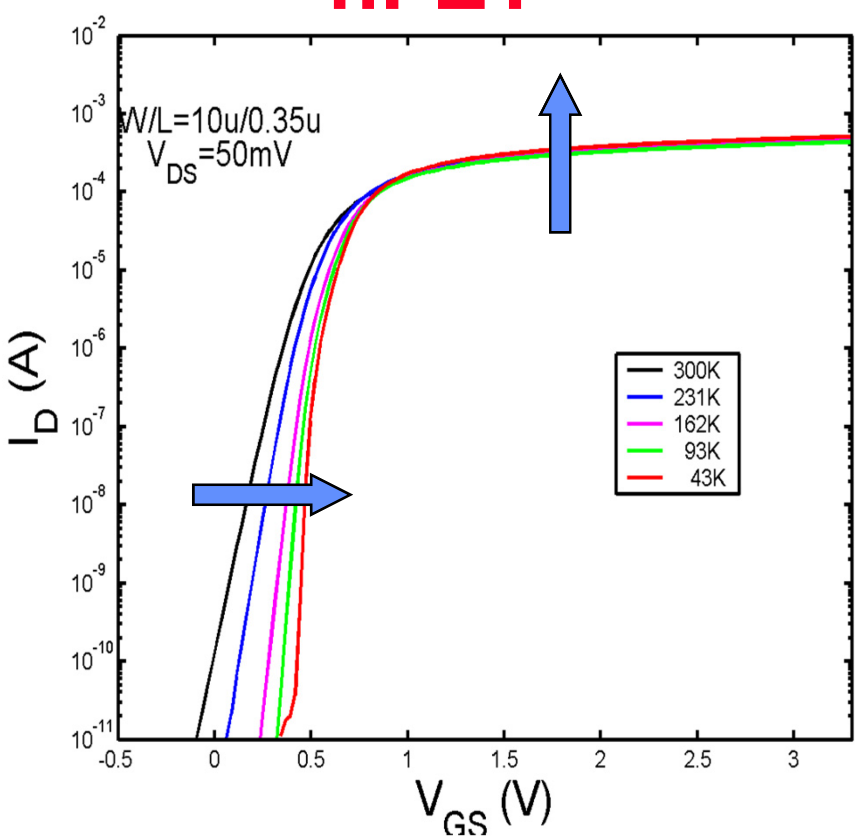
➢ **CB stability analysis used to examine various pinch-in influences**

Cryogenic Operation of CMOS

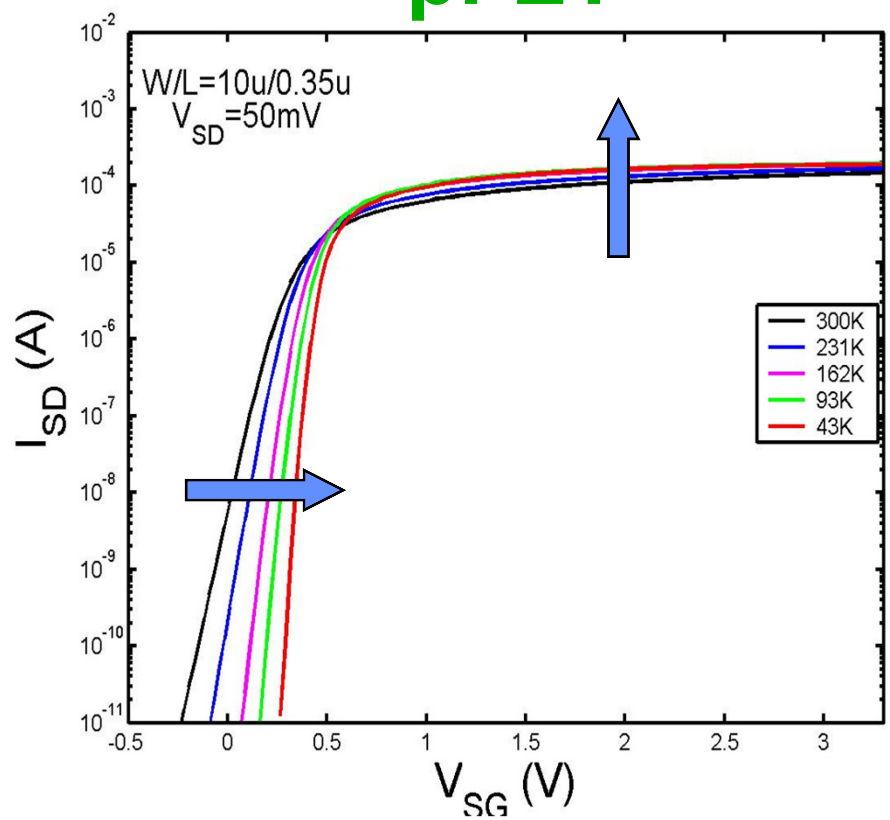
Sub-Threshold Behavior

- First Generation SiGe BiCMOS (0.35 um L_{eff})
- V_T and Subthreshold Swing Increase with Cooling
- Output Drive Improves with Cooling

nFET



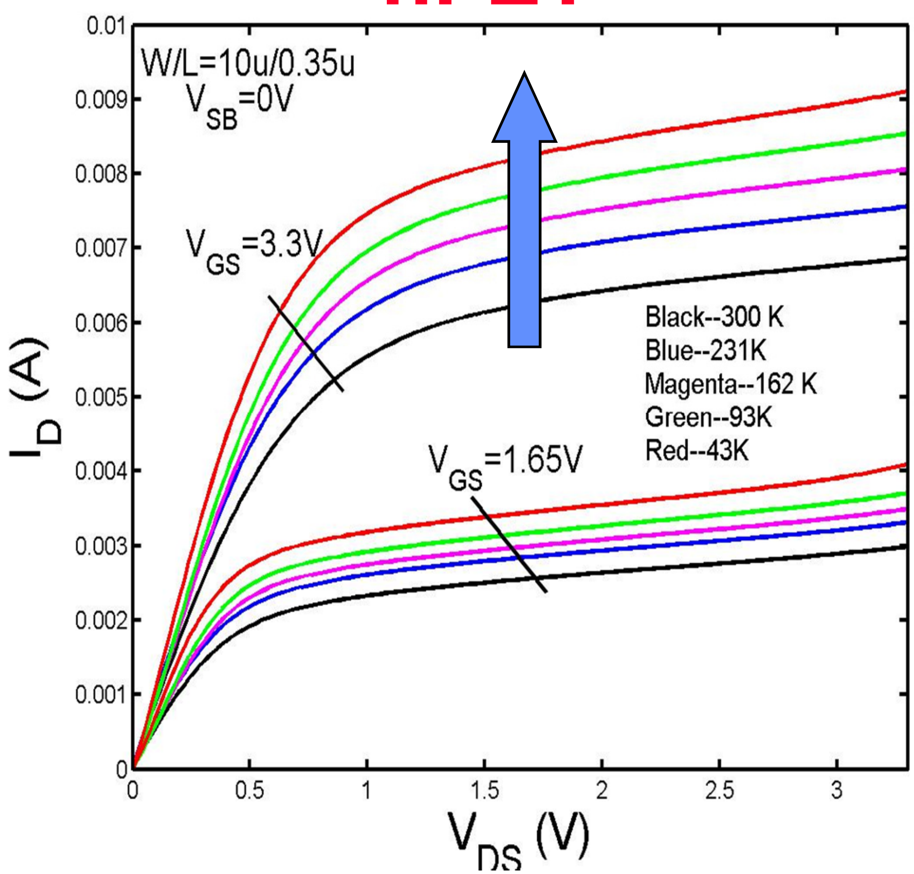
pFET



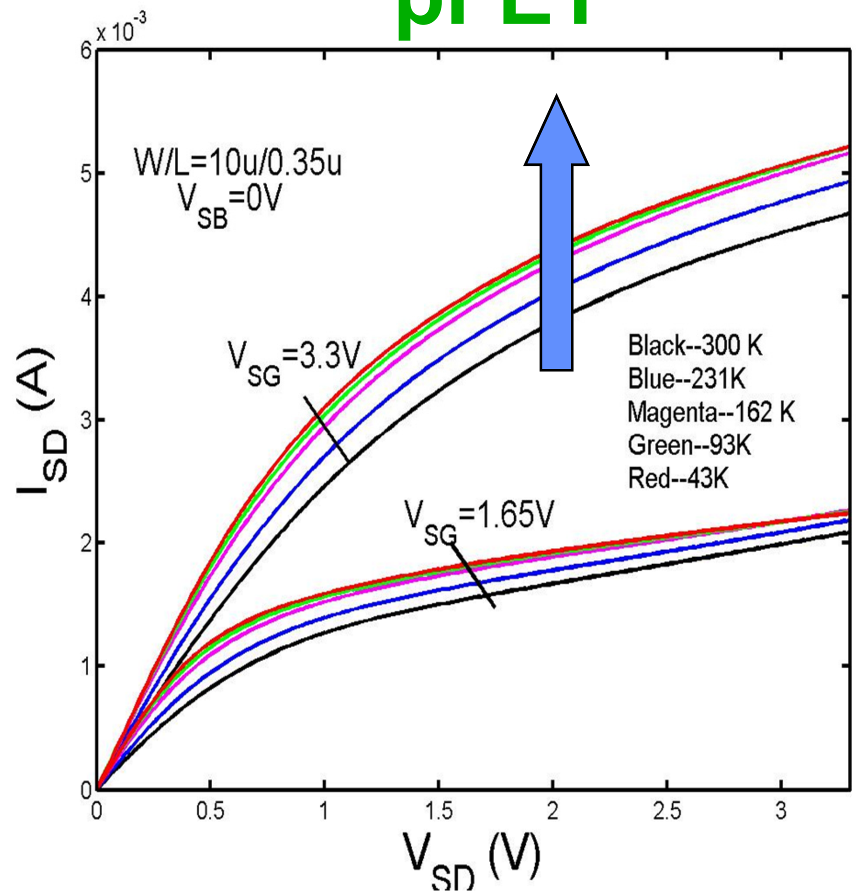
Output Characteristics

- **Improved Current Drive With Cooling**
- **Modest Degradation in Output Conductance**

nFET

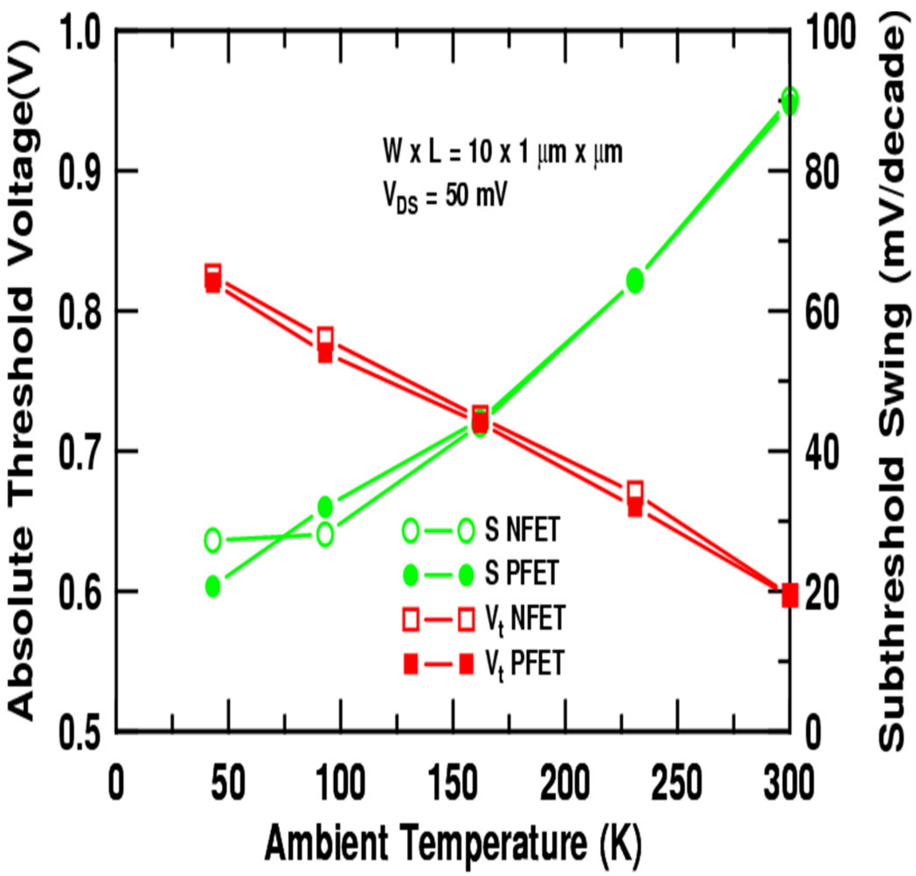


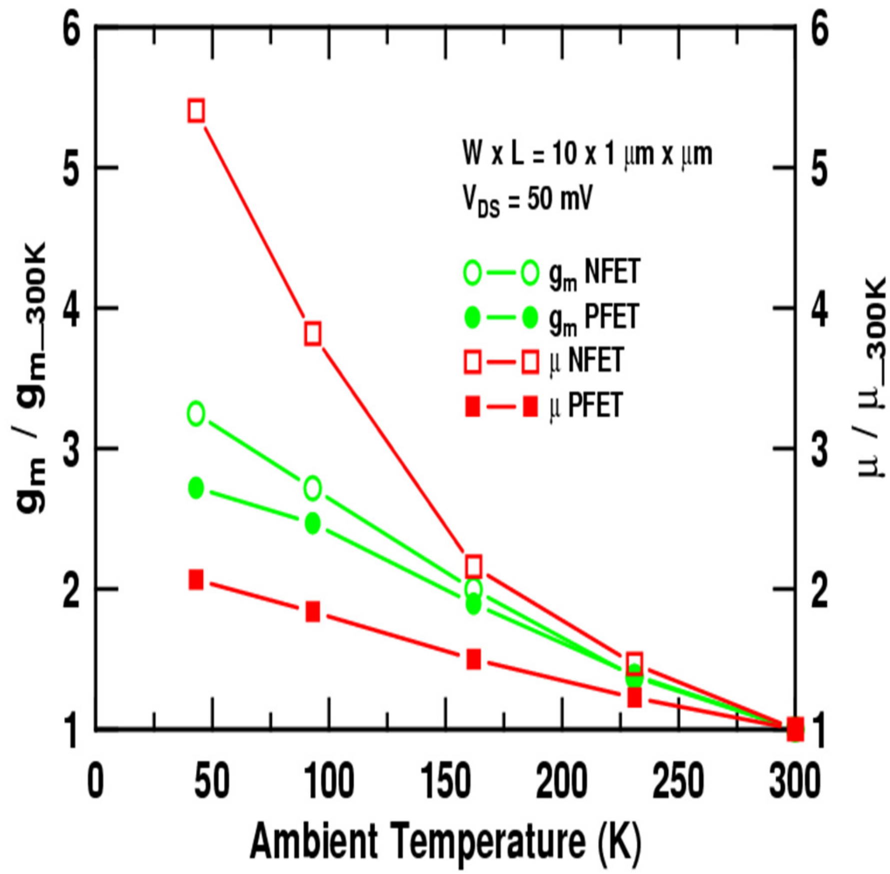
pFET



T Dependence

- V_T Increases with Cooling / S Decreases with Cooling
- g_m Increases with Cooling / μ Increases with Cooling

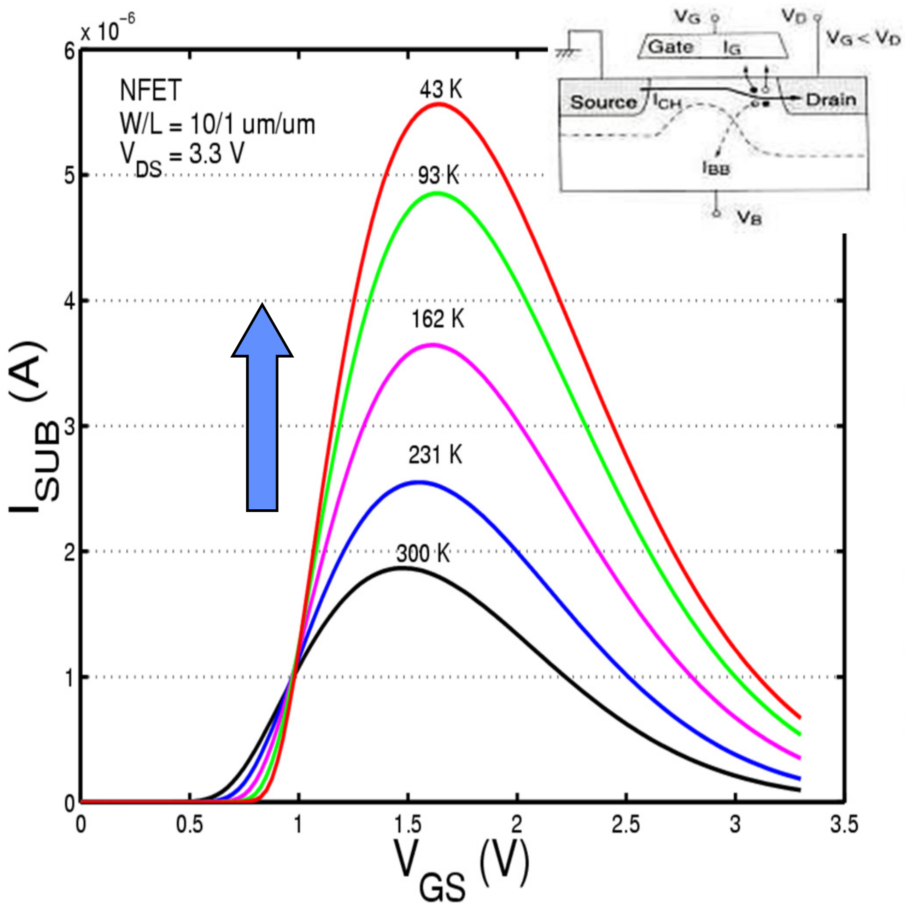


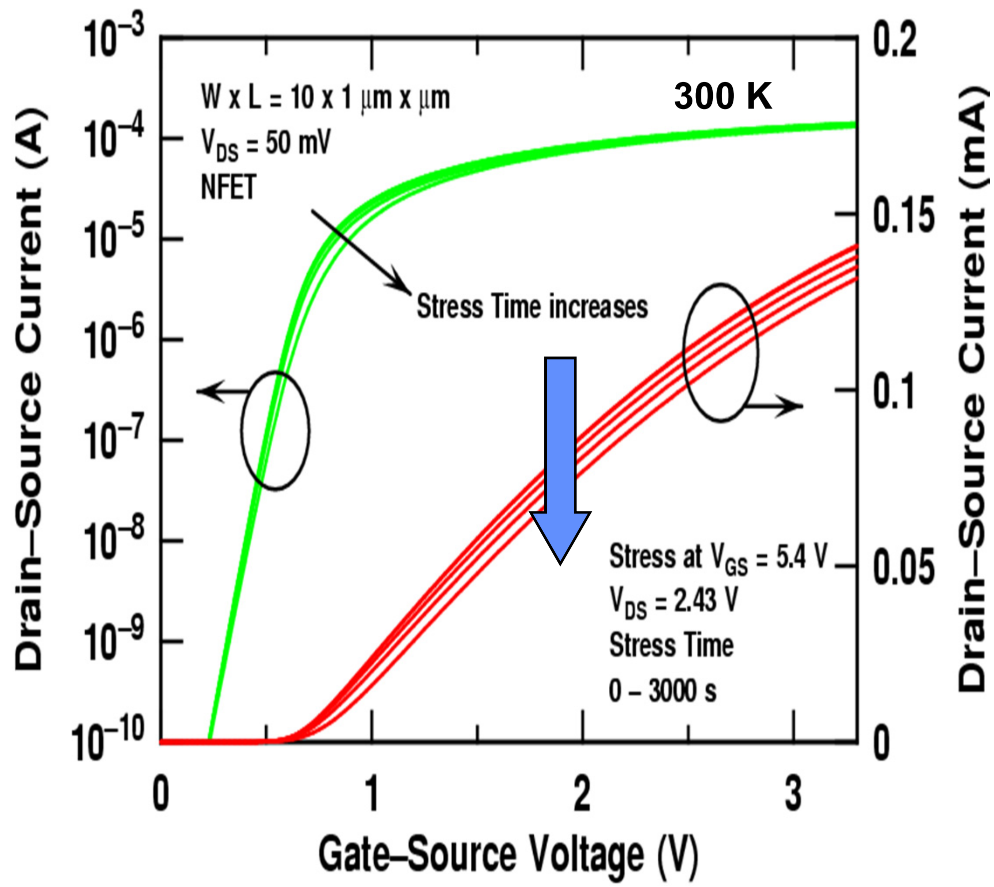


How About Reliability?

Device Reliability

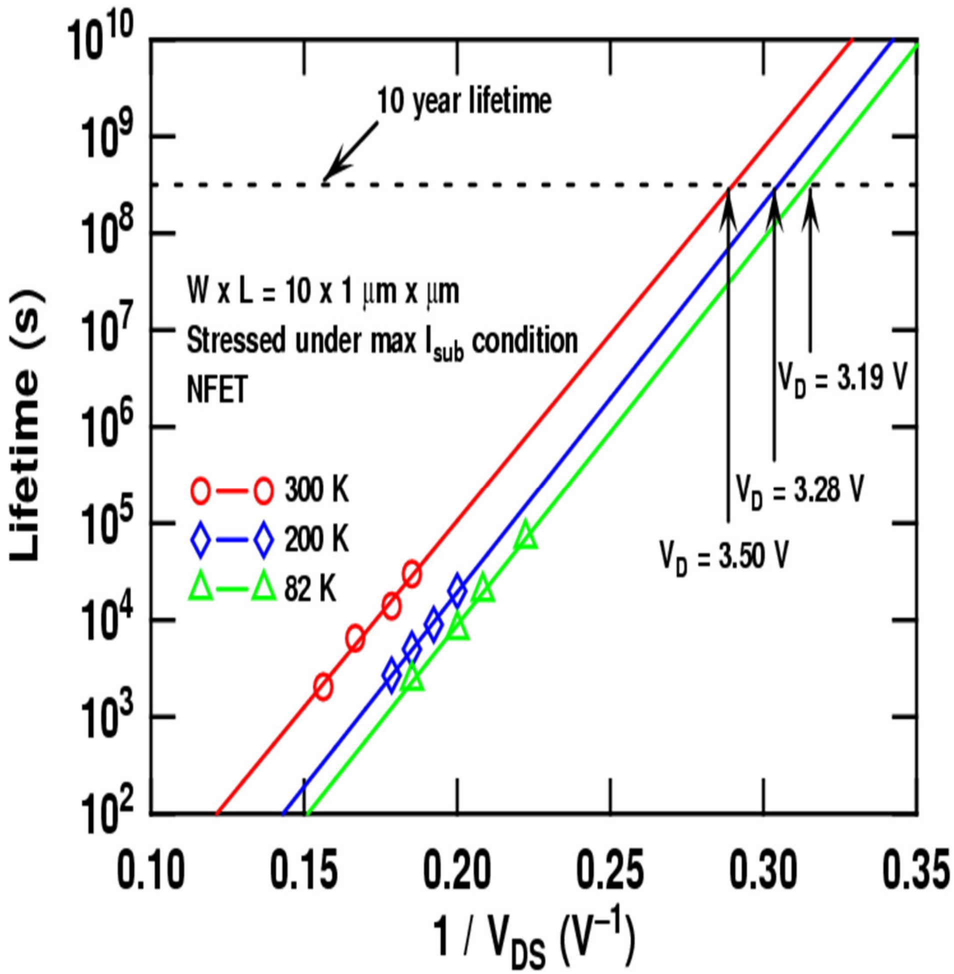
- I_{SUB} is a Good Monitoring Parameter for HCE
- After Stress, I_d and g_m Decrease While V_T and S Increase

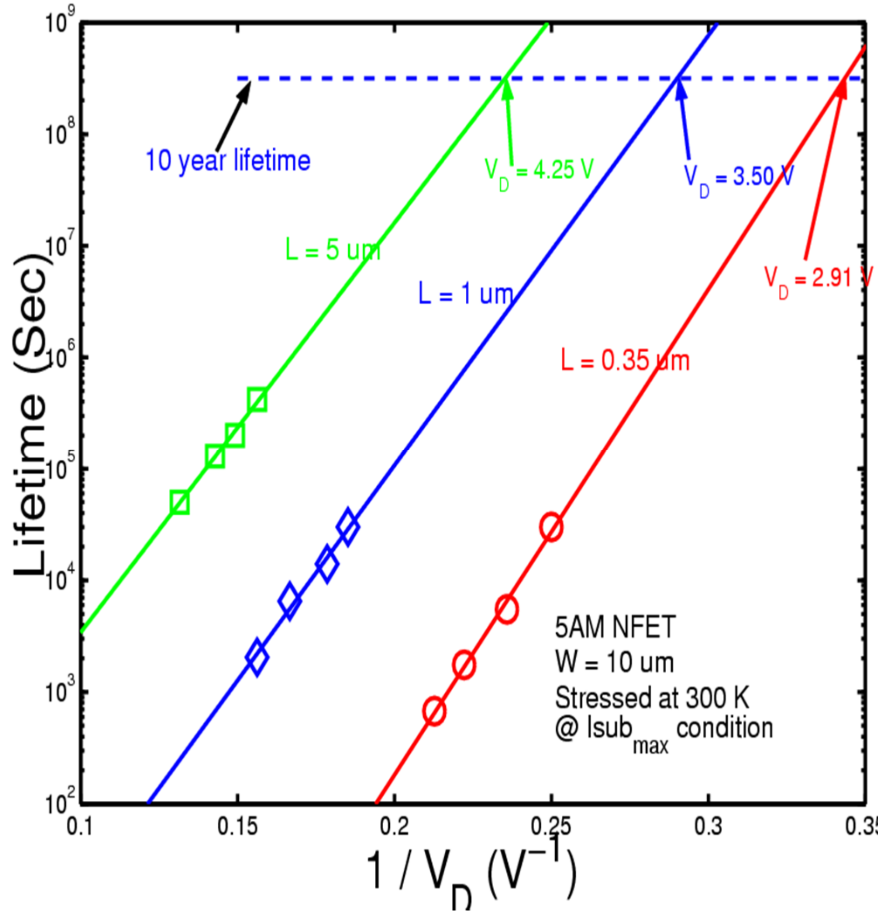




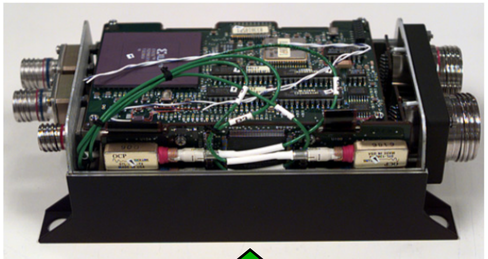
MOSFET L,T Dependence

- **Lifetime Decreases with Cooling at Fixed L**
- **Lifetime Decreases with L at Fixed T (Mitigation Path)**

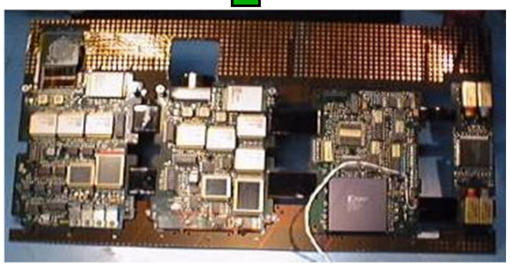




Remote Electronics Unit

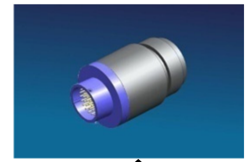


The X-33 Remote Health Unit, circa 1998



SiGe

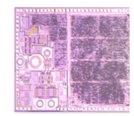
The ETDP Remote Electronics Unit, circa 2009

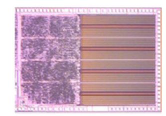


REU in connector housing!

Analog front end die

Digital control die





Conceptual integrated REU system-on-chip SiGe BiCMOS die

Specifications

- 5” x 3” x 6.75” = 101 in^3
- 11 kg
- 17 Watts
- -55^{o}C to +125^{o}C

Goals

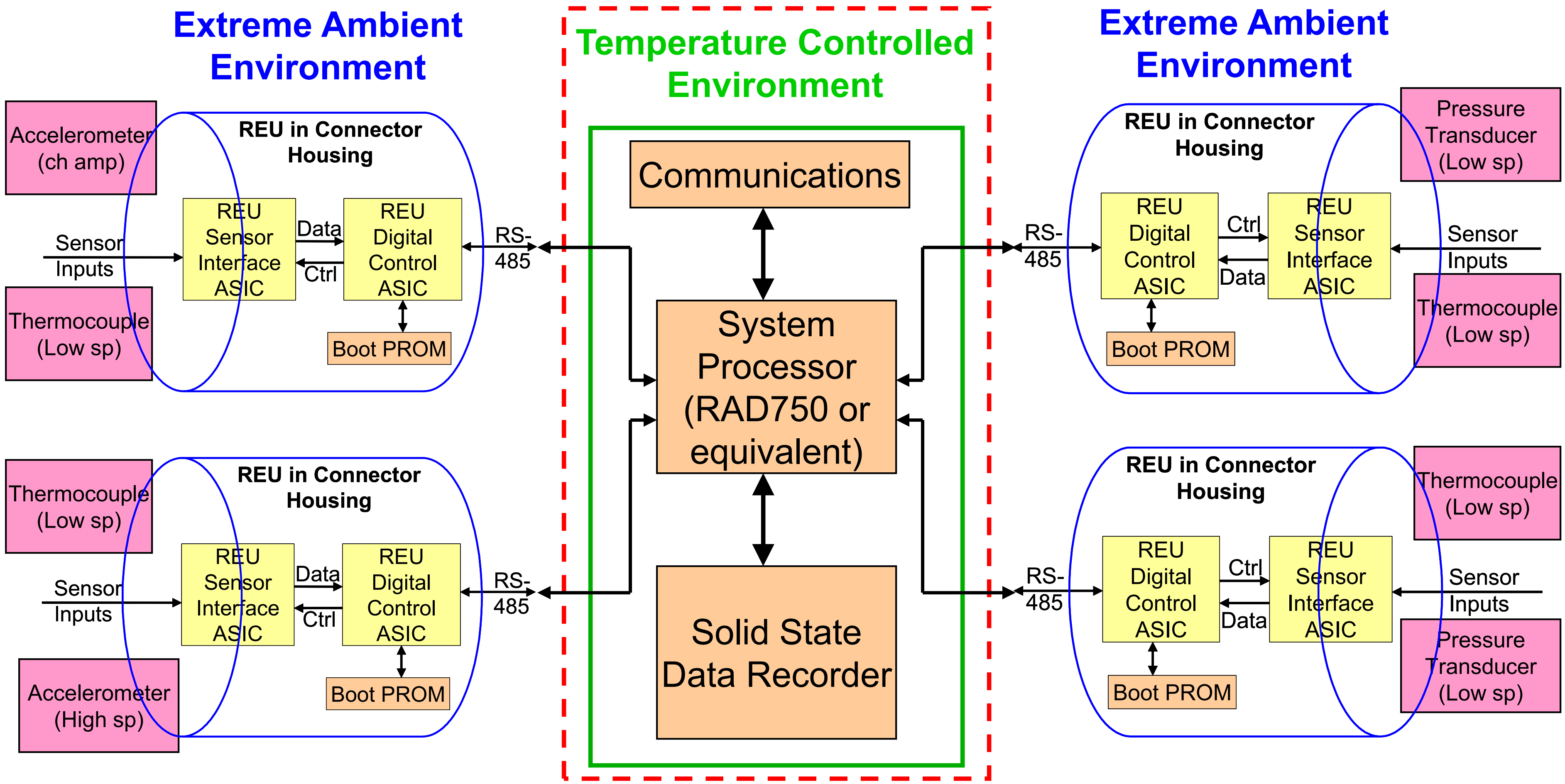
- 1.5” x 1.5” x 0.5” = 1.1 in^3 **(100x)**
- < 1 kg **(10x)**
- < 2 Watts **(10x)**
- **-180^{o}C to +125^{o}C, rad tolerant**

Supports Many Sensor Types:

Temperature, Strain, Pressure, Acceleration, Vibration, Heat Flux, Position, etc.

Use This REU as a Remote Vehicle Health Monitoring Node

SiGe REU Architecture



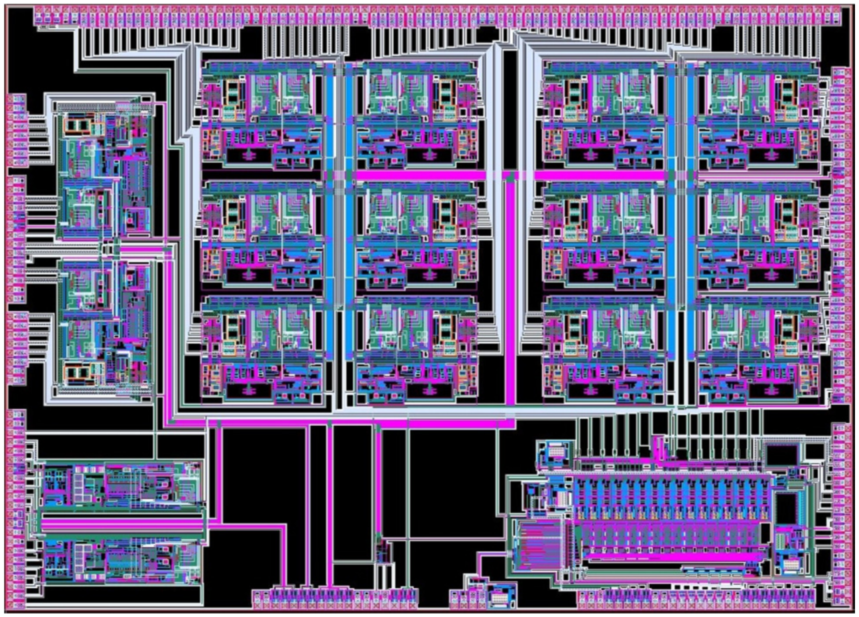
Major Advantages:

- **Eliminates Warm Box** (size, weight, and power; allows de-centralized architecture)
- **Significant Wiring Reduction** (weight, reliability, simplifies testing & diagnostics)
- **Commonality** (easily adapted from one system to the next)

RSI Chip for REU

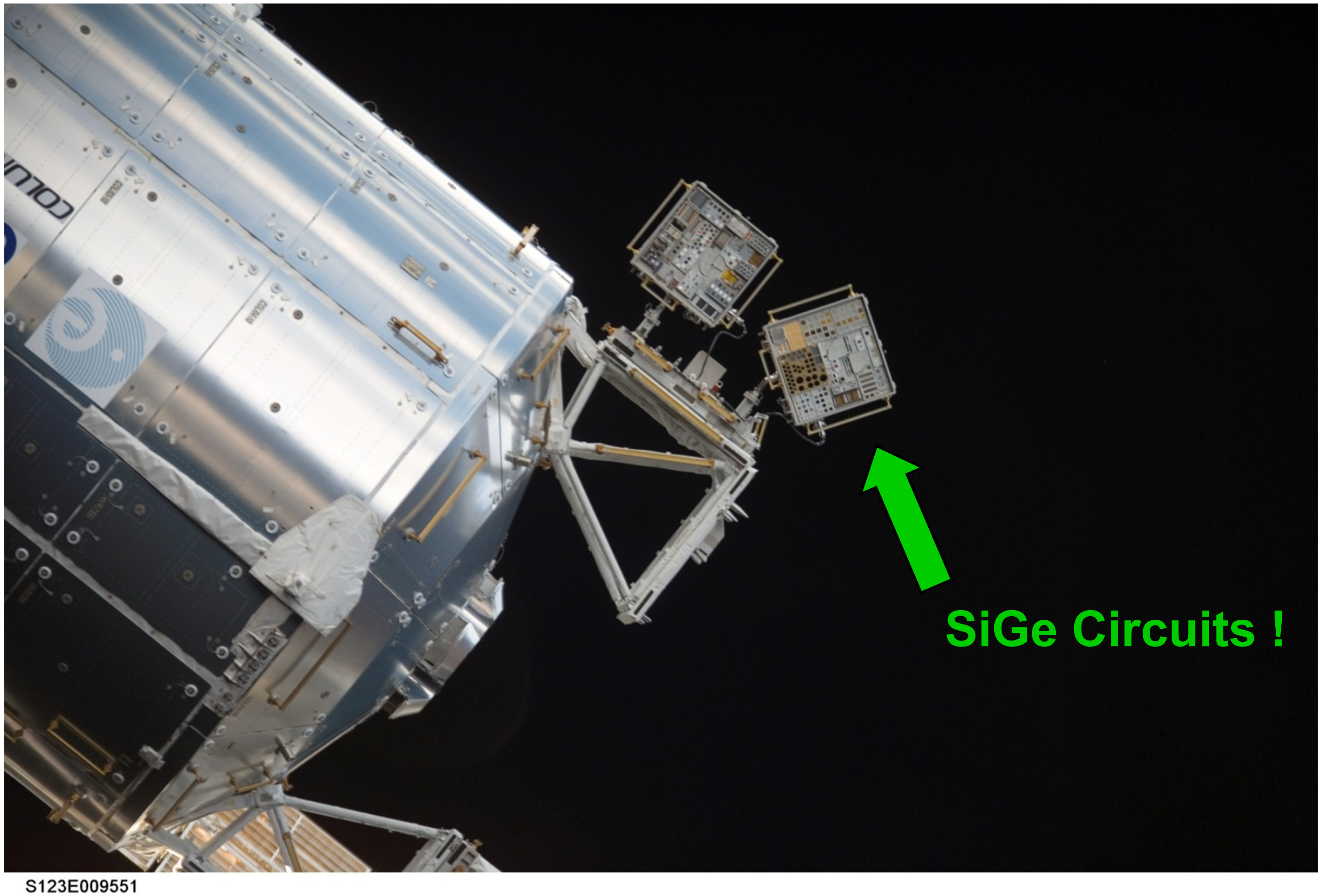
❑ RSI (CRYO-5a):

- **16-channel monolithic Remote Electronics Unit Sensor Interface (RSI) ASIC**
- **10 mm x 14 mm**
- **Current I/O estimate 236 I/O**
  - 139 signal I/O
  - 50 ESD
  - 40 power I/O
  - 7 explicit test I/O
- **Top-Level cells:**
  - UT – (1) 12-bit 16-channel Wilkinson ADC
  - UARK – (12) Low-speed Channels
  - AU – (2) High-speed channels
  - GT – (2) Charge-amp channels
  - UT – (1) Flying capacitor 6-phase clock generator



CRYO-5A 10x14 mm^2

MISSE-6 ISS Mission



Recent NASA photograph of MISSE-6 after deployment, taken by the Space Shuttle Crew

Ultra Low Power Mixed-Signal Design Challenges for Moon

Ben Blalock
Integrated Circuits & Systems Laboratory
The University of Tennessee

November 3, 2010

Some Perspective…

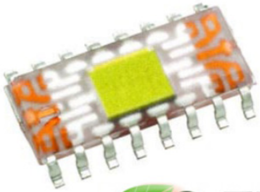
- **Battery life with 1 µA:**

With 1.2 µA supply current, 30 mAh battery can continuously supply for 5 years!

From 30 mAh to 600 mAh

>> 600 mAh

Solar: endless

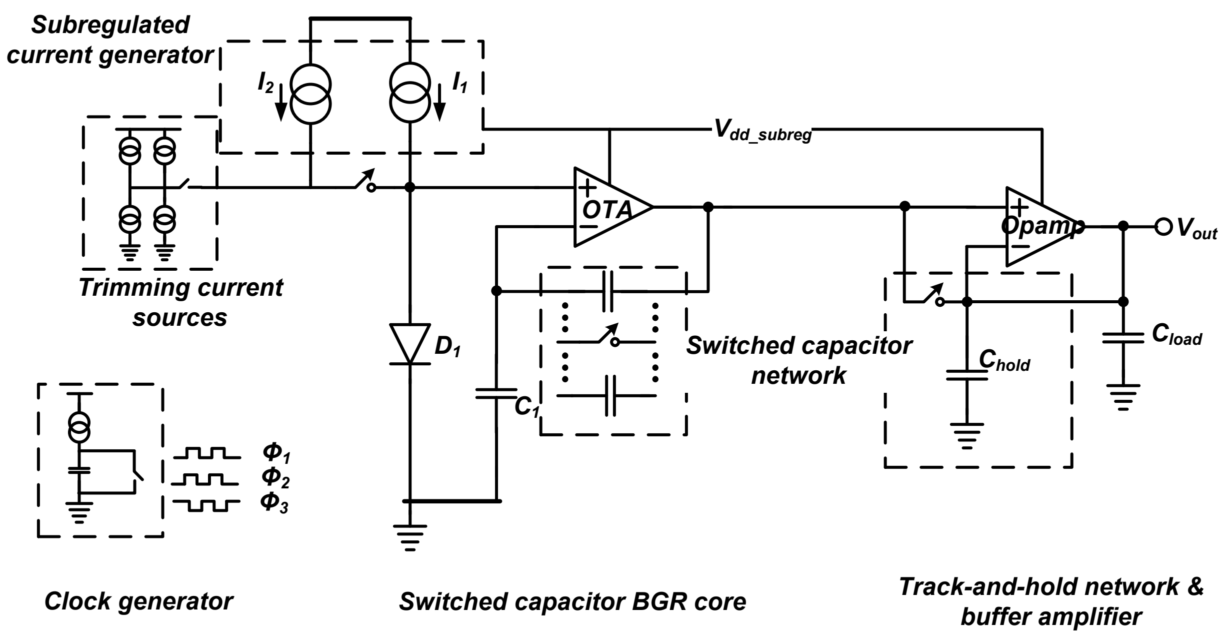


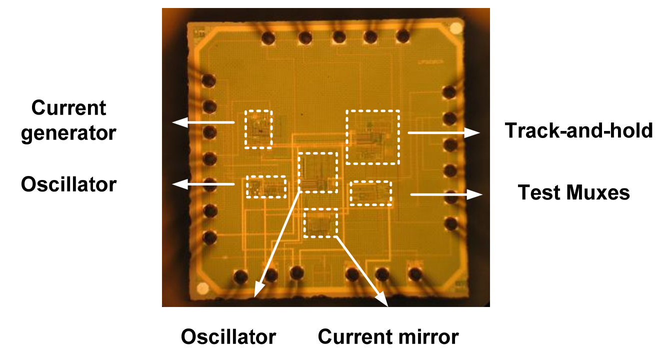
Clare CPC1832
I_{OUT} = 50 µA

IXYS SOLAR
Efficiency By The Sun

What 1 µA can do?

- Quite a bit—thanks to ultra low power IC design
- E.g., Swithed Capacitor Voltage Reference running on 1 µA:





Not designed for cold temperature...

S. Chen and B. J. Blalock, "Analog Circuits for Nano-Power Applications," submitted to *IEEE Transactions on Circuits and Systems II*.

Ultra Low Power Circuit Design

- Subthreshold (weak inversion) operation has been heavily utilized to accommodate bias current scaling to reduce power
- MOSFET in Weak Inversion:
  - Transconductance efficiency (g_m/I_D) is at a maximum
    - Speed/Watt or precision/Watt is maximized
  - Low value of V_{DSAT} (≈ 0.1V) required for saturation enables lower V_{DD}
  - Velocity saturation is non-existent in subthreshold designs
  - Carrier heating effects that lead to noise & degradation of I_D are avoided
  - Subthreshold exponential I_D relation can be leveraged to implement analog computation systems
  - But… High g_m/I_D ratio and exponential dependency of I_D on voltage and temperature results in high sensitivity to transistor mismatch (at least 2X worse) and temperature

Challenges and Future Work

Ultra-Low Power Low Temperature Electronics

- Ultra low power vs. temperature
  - Present design techniques call for reduction of the supply voltage; however:
    - MOSFET threshold voltages increase as temperature decreases.
    - BJT (SiGe) V_{be} increases as temperature decreases.
- This means for the same signal strength, we need larger supply voltage at lower temperatures.
- Industry trend is supply voltage reduction: 5V to 3.3V to 1.2V to 0.8V…

Challenges and Future Work

Instrument Quality, Low Noise and Low Power Electronics

- Precision low noise electronics vs. power and temperature
  - Precision electronics need large voltage headroom
  - Precision electronics use high bias current to reduce device noise
- Combination of current and voltage means power…

Digital Electronics-Synchronous Machines

- Field programmable Gate Arrays
  - Reduced clock speed to avoid signal collision
  - ACTEL FPGA’s can operate to -180C. Xilinx FPGA’s have cold start problem at T<-60C (Use micro heater as a starter)
  - SRAMs can operate to -180C
  - DRAM (high density) do not operate at -180C due to readout circuits. Ben can fix this in a jiffy.
  - Flash memory not tested for Lunar temp

  Revolutionary ideas:

  Asynchronous computing

  Adiabatic computing